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APPLICATION FOR LETTERS PATENT

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CIRCUITRY COMPRISING ROUGHENED
PLATINUM LAYERS, PLATINUM-CONTAINING
MATERIALS, CAPACITORS COMPRISING
ROUGHENED PLATINUM LAYERS, METHODS
OF FORMING ROUGHENED LAYERS OF
PLATINUM, AND METHODS OF FORMING
CAPACITORS

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1 CIRCUITRY COMPRISING ROUGHENED PLATINUM LAYERS,
2 PLATINUM-CONTAINING MATERIALS
3 CAPACITORS COMPRISING ROUGHENED PLATINUM LAYERS,
4 METHODS OF FORMING ROUGHENED LAYERS OF PLATINUM,
5 AND METHODS OF FORMING CAPACITORS

6 TECHNICAL FIELD

7 The invention pertains to methods of forming and using platinum-
8 containing materials, and to circuitry incorporating roughened layers of
9 platinum.

10 BACKGROUND OF THE INVENTION

11 Platinum is a candidate for utilization as a conductive material in
12 advanced semiconductor processing. Platinum can be utilized in an
13 elemental form, or as an alloy (such as, for example, rhodium/platinum),
14 and can be deposited onto a substrate by, for example, sputter deposition
15 or chemical vapor deposition (CVD) methods. Platinum is typically
16 formed to have a relatively smooth upper surface. Such smooth upper
17 surface can be advantageous in, for example, applications in which
18 circuitry is formed over the platinum layer. Specifically, the relatively
19 smooth surface can provide a substantially planar platform upon which
20 other circuitry is formed. However, there can be advantages to
21 incorporating roughened conductive layers into integrated circuitry in
22 applications where high surface area is desired, as with capacitor

1 electrodes. Accordingly, it would be desirable to develop methods of
2 forming platinum layers having roughened outer surfaces.

3 In another aspect of the prior art, platinum-comprising materials
4 are frequently utilized as catalysts in, for example, the petroleum
5 industry, as well as in, for example, automobile exhaust systems.
6 Frequently, an efficiency of a catalyst can be improved by enhancing a
7 surface area of the catalyst. Accordingly, it would be desirable to
8 develop methods of enhancing surface area of platinum-comprising
9 materials.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a roughened layer of platinum. A substrate is provided within a reaction chamber. An oxidizing gas is flowed into the reaction chamber, and a platinum precursor is flowed into the chamber. Platinum is deposited from the platinum precursor over the substrate in the presence of the oxidizing gas. A temperature within the chamber is maintained at from about 0°C to less than 300°C during the depositing.

In another aspect, the invention encompasses a circuit comprising a roughened platinum layer over a substrate. The roughened platinum layer has a continuous surface characterized by columnar pedestals.

In yet another aspect, the invention encompasses a platinum catalyst characterized by a continuous outer surface portion of the platinum having a plurality of columnar pedestals that are at least about 400Å tall. The surface portion covers an area that is at least about 4×10^6 square Angstroms.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, fragmentary, cross-sectional view of a semiconductive wafer fragment processed according to a method of the present invention.

1 Fig. 2 is a fragmentary top view of the semiconductor wafer
2 fragment of Fig. 1.

3 Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step
4 subsequent to that of Fig. 1.

5 Fig. 4 is a scanning electron microscope (SEM) micrograph of a
6 platinum film produced by CVD of $\text{MeCpPt}(\text{Me})_3$.

7 Fig. 5 is a SEM micrograph of a platinum film produced by CVD
8 of $\text{MeCpPt}(\text{Me})_3$ under different conditions than those utilized for
9 forming the film of Fig. 4.

10 11 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

12 This disclosure of the invention is submitted in furtherance of the
13 constitutional purposes of the U.S. Patent Laws "to promote the progress
14 of science and useful arts" (Article 1, Section 8).

15 The invention encompasses methods of forming platinum layers
16 having roughened outer surfaces, and methods of incorporating such
17 layers into capacitor constructions. Fig. 1 shows a semiconductor wafer
18 fragment 10 at a preliminary processing step of the present invention.
19 Wafer fragment 10 comprises a substrate 12. Substrate 12 can comprise,
20 for example, a monocrystalline silicon wafer lightly doped with a
21 background p-type dopant. To aid in interpretation of the claims that
22 follow, the term "semiconductive substrate" is defined to mean any
23 construction comprising semiconductive material, including, but not limited

1 to, bulk semiconductive materials such as a semiconductive wafer (either
2 alone or in assemblies comprising other materials thereon), and
3 semiconductive material layers (either alone or in assemblies comprising
4 other materials). The term "substrate" refers to any supporting
5 structure, including, but not limited to, the semiconductive substrates
6 described above.

7 A diffusion region 14 is formed within substrate 12 and defines a
8 node location to which electrical connection with a storage node of a
9 capacitor is to be made. Diffusion region 14 can be formed by, for
10 example, implanting a conductivity enhancing dopant into substrate 12.

11 An adhesion layer 16 is formed over substrate 12 and in electrical
12 contact with diffusion region 14, and a platinum-comprising layer 18 is
13 formed over adhesion layer 16. Adhesion layer 16 is provided to
14 enhance adhesion of platinum-comprising layer 18 to substrate 12. In
15 other embodiments (not shown) a platinum-comprising layer can be
16 provided directly onto a silicon surface (either the monocrystalline silicon
17 surface of substrate 12, or an intervening amorphous or polycrystalline
18 surface). Such embodiments are less preferred than the shown
19 embodiment due to difficulties of adequately adhering platinum directly
20 to silicon.

21 Adhesion layer 16 can comprise, for example, at least one of
22 titanium nitride, iridium, rhodium, ruthenium, platinum, palladium,
23 osmium, silver, rhodium/platinum alloy, IrO_2 , RuO_2 , RhO_2 , or OsO_2 .

1 Adhesion layer 16 can be formed by, for example, chemical vapor
2 deposition, and can be formed to a thickness of, for example, less
3 than 100Å.

4 Platinum-comprising layer 18 can comprise, for example, elemental
5 platinum, or a platinum alloy, such as rhodium/platinum alloy. Platinum-
6 comprising layer 18 is provided to have a roughened outer surface 20.
7 Such can be accomplished by chemical vapor deposition of platinum-
8 comprising layer 18 under relatively low temperature conditions, and in
9 the presence of an oxidizing atmosphere. For instance, a platinum-
10 comprising layer 18 formed as follows will comprise a roughened outer
11 surface 20.

12 First, substrate 12 is inserted within a CVD reaction chamber. An
13 oxidizing gas and a platinum precursor are flowed into the reaction
14 chamber. Platinum is deposited from the platinum precursor over
15 substrate 12 in the presence of the oxidizing gas. A temperature within
16 the reaction chamber is maintained at from about 0°C to less than
17 300°C during the depositing, and a pressure within the reactor is
18 preferably maintained at from about 0.5 Torr to about 20 Torr. Suitable
19 control of the temperature and of a relative flow rate of the oxidizing
20 gas to the platinum precursor causes deposited platinum layer 18 to have
21 a roughened outer surface 20. The platinum precursor is flowed into
22 the reaction chamber in a carrier gas, such as, for example, a gas known
23 to be generally inert to reaction with platinum precursor materials, such

1 as, for example, helium or argon. The platinum precursor can comprise,
2 for example, at least one of MeCpPtMe_3 , CpPtMe_3 , $\text{Pt}(\text{acetylacetonate})_2$,
3 $\text{Pt}(\text{PF}_3)_4$, $\text{Pt}(\text{CO})_2\text{Cl}_2$, $\text{cis}[\text{PtMe}_2(\text{MeNC})_2]$, or platinum
4 hexafluoroacetylacetonate; wherein Cp is a cyclopentadienyl group and Me
5 is a methyl group. The oxidizing gas can comprise, for example, at least
6 one of O_2 , N_2O , SO_3 , O_3 , H_2O_2 , or NO_x , wherein x has a value of
7 from 1 to 3. In embodiments wherein platinum layer 18 comprises a
8 platinum/metal alloy, at least one other metal precursor can be flowed
9 into the reaction chamber to deposit the platinum as an alloy of the
10 platinum and the at least one other metal. The at least one other
11 metal precursor can comprise, for example, a precursor of rhodium,
12 iridium, ruthenium, palladium, osmium, and/or silver.

13 The oxidizing gas can assist in deposition of platinum from the
14 platinum-comprising precursor by oxidizing carbon from the precursor
15 during deposition of the platinum. Also, the oxidizing gas can influence
16 a deposition rate of a platinum-comprising layer. Specifically, a greater
17 rate of flow of the oxidizing gas relative to the flow of the platinum
18 precursor can lead to faster deposition of the platinum-comprising layer.
19 The rate of flow of platinum precursor is influenced by a rate of flow
20 of carrier gas through a liquid organic precursor solution, and by a
21 temperature of the precursor solution. In preferred embodiments of the
22 invention, a carrier gas will be flowed through a liquid organic precursor
23 solution at a rate of from about 2 sccm to about 1000 sccm and more

1 preferably at less than or equal to about 30 sccm. In such preferred
2 embodiments, the oxidizing gas will be flowed at a flow rate of at least
3 about 50 sccm. The organic precursor will preferably be at a
4 temperature of from about 0°C to about 100°C, and more preferably
5 from about 30°C to about 50°C.

6 A rate of growth of platinum-comprising layer within the reaction
7 chamber is also influenced by a temperature of the substrate.
8 Specifically, if platinum is deposited under conditions wherein the
9 temperature of the substrate is maintained at from about 220°C to less
10 than 300°C, the platinum will deposit at a rate of about 600Å in
11 about 30 seconds. If a temperature of the substrate is reduced to below
12 about 210°C, a rate of deposition of platinum will decrease considerably.
13 It is preferred that a deposition time for a 600Å thick platinum-
14 comprising layer be less than or equal to about 40 seconds to maintain
15 efficiency of a production process. Accordingly, it is preferred that the
16 temperature of the substrate be maintained at above about 210°C, and
17 preferably at from greater than or equal to about 220°C during
18 deposition of the platinum-comprising layer within the reaction chamber.

19 It is also found that if a temperature is greater than 300°C and
20 less than about 350°C, a deposited platinum layer will have a smooth
21 outer surface, rather than a desired roughened outer surface. Further,
22 if the temperature of the substrate exceeds about 400°C, a deposited
23 platinum surface will have holes extending to a surface underlying the

1 platinum surface, rather than being a continuous surface overlying a
2 substrate. Accordingly, it is preferred that the temperature of the
3 substrate be well below 400°C, more preferred that the temperature be
4 below 300°C, and even more preferred that the temperature be less than
5 or equal to about 280°C. In preferred embodiments of the present
6 invention, the temperature of the substrate will be maintained at from
7 about 220°C to about 280°C, whereupon it is found that a platinum
8 layer having a roughened outer surface can be deposited to a thickness
9 of about 600Å in about 30 seconds.

10 Platinum layer 18 is preferably deposited to a thickness of at least
11 about 400Å to avoid having surface anomalies (such as crevices or holes)
12 that extend entirely through layer 18 to an underlying layer, and is
13 preferably deposited to a thickness of at least about 600Å. However, in
14 some embodiments holes extending entirely through layer 18 will be of
15 little or no consequence in semiconductor circuitry ultimately formed
16 from layer 18. Such embodiments can include, for example, embodiments
17 wherein adhesion layer 16 is provided beneath platinum-comprising
18 layer 18. Accordingly, in embodiments wherein platinum layer 18 is
19 provided over an adhesion layer 16, it can be preferred to provide
20 platinum layer 18 to a thickness of less than 400Å because of space
21 limitations due to the close packing of capacitors. Also, in embodiments
22 in which platinum layer 18 is utilized in forming circuitry having tight
23 spacing requirements it can be preferred to form layer 18 to be

1 relatively thin. For instance, in some capacitor constructions it can be
2 desired to form layer 18 to be less than or equal to about 1000Å, and
3 more preferred to form layer 18 to be from about 300Å to about 400Å
4 to avoid electrical contact between adjacent capacitor structures.

5 A fragmentary top view of wafer fragment 10 is shown in Fig. 2.
6 Layer 18 is preferably a continuous layer (defined as a layer without
7 cavities extending therethrough to an underlying layer -- such as the
8 underlying layer 16 of Fig. 2) across its entirety. Alternatively, some
9 portion of layer 18 is continuous. For example, consider an application
10 where layer 18 overlies and contacts a conductive layer to form a circuit
11 device comprising both layer 18 and the underlying conductive layer. In
12 such applications, it is generally still desired that a substantial portion
13 of layer 18 be continuous to, for example, maintain a uniform electrical
14 contact between layer 18 and the underlying conductive layer. Such
15 substantial portion will preferably cover a surface area of at least about
16 4×10^6 square Angstroms. A surface area of about 4×10^6 square
17 Angstroms is illustrated in Fig. 3 as a square 50 having sides of about
18 2000 Angstroms.

19 Fig. 3 illustrates an embodiment wherein platinum-comprising
20 layer 18 is incorporated into a capacitor construction 30 as a storage
21 node. Specifically, a dielectric layer 22 and a capacitor electrode 24 are
22 provided over platinum-comprising layer 18 to form capacitor
23 construction 30. Dielectric layer 22 can comprise one or more of silicon

oxide or silicon nitride, or it can comprise other dielectric materials, such as, for example, tantalum pentoxide, or BaSrTiO_3 . Capacitor electrode 24 can comprise, for example, TiN, conductively doped silicon (such as polysilicon), or a metal, such as, for example, platinum. In embodiments wherein capacitor electrode 24 comprises platinum, capacitor electrode 24 can be formed by chemical vapor deposition over dielectric layer 22. The chemical vapor deposition can be conducted either to form upper electrode 24 with a relatively smooth upper surface, or to form upper electrode 24 with a relatively rough upper surface. If capacitor electrode 24 is to be formed of platinum with a relatively smooth upper surface, it can be chemical vapor deposited in a reaction chamber with a temperature maintained at above about 300°C and/or with an oxidizing gas flow rate of less than 50 sccm and a carrier gas flow rate of greater than 30 sccm. Also, any platinum comprised by capacitor electrode 24 can be in the form of elemental platinum, or an alloy, such as, for example, rhodium/platinum alloy.

As shown, layer 18 has a rough outer surface and layers 22 and 24 are conformal to the rough outer surface of layer 18.

Figs. 4 and 5 illustrate scanning electron microscope (SEM) micrographs of platinum films produced by CVD of $\text{MeCpPt}(\text{Me})_3$. Fig. 4 illustrates a surface produced within a reaction chamber in a time of about 6 minutes, wherein a temperature in the chamber was about 215°C , a pressure was about 5 Torr, a flow rate of carrier gas

(He, with a pressure at the carrier gas bubbler of about 6 Torr) was about 5 sccm, and a flow rate of oxidizing gas (O_2) was about 50 sccm. The platinum surface formed comprises pedestals characteristic of columnar growth. The columnar pedestals terminate in dome-shaped (substantially hemispherical) tops. It can be advantageous to have substantially hemispherical tops, rather than tops having sharp edges, in forming capacitor constructions or other electronic circuitry from a deposited platinum layer. Specifically, the relatively rounded hemispherical surfaces can create relatively uniform electric fields at the surface of a deposited platinum layer. In contrast, if sharp edges were present, the sharp edges could form loci for high electric fields, and lead to leakage of electric current across the capacitor. The platinum layer illustrated in Fig. 4 can be referred to as "hemispherical grain" platinum to indicate a structure largely analogous to a material known in the art as hemispherical grain polysilicon.

The platinum layer of Fig. 4 is characterized by columnar pedestals generally having heights greater than or equal to about one-third of a total thickness of the platinum layer. Many of the pedestals shown in Fig. 4 have a height approximately equal to a thickness of the deposited platinum layer. Accordingly, if the deposited platinum layer has a thickness of about 600\AA , the individual pedestals can have a thickness approaching 600\AA . Such is only an approximation to the size of the pedestals as it is found that some of the pedestals will grow from

1 surfaces of other pedestals, and some of the pedestals will grow less
2 vertically than other pedestals. An average diameter of the pedestals is
3 about 200Å, and the pedestals are generally closely packed (i.e., the
4 pedestals generally touch other pedestals and many pedestals fuse with
5 other pedestals), but the distribution of the pedestals is typically not a
6 close-packed structure (i.e., a structure wherein all the pedestals are
7 tightly packed in, for example, an hexagonal type arrangement to form
8 a maximum number of pedestals on a given surface). The columnar
9 growth illustrated in Fig. 4 is found not to occur if a temperature within
10 a CVD reaction chamber is above 300°C.

11 Fig. 5 illustrates a surface produced on a platinum film within a
12 reaction chamber in a time of about 150 seconds, wherein a temperature
13 in the chamber was 300°C, a pressure was about 0.5 Torr, a flow rate
14 of carrier gas (He, with a pressure at the carrier gas bubbler of
15 about 6 Torr) was about 30 sccm, and a flow rate of oxidizing gas (O₂)
16 was about 10 sccm. The platinum layer deposited under the Fig. 5
17 conditions has a much smoother surface than that deposited under the
18 Fig. 4 conditions. Figs 4 and 5 together evidence that it is possible to
19 control a grain structure of a surface of a chemical vapor deposited
20 platinum layer by controlling process parameters of a chemical vapor
21 deposition reaction chamber.

22 Although the invention has been described with application to
23 formation of a capacitor structure, it is to be understood that the

1 invention can be utilized in a number of other applications as well. For
2 instance, a platinum layer having a roughened surface can be utilized for
3 formation of catalysts.

4 In compliance with the statute, the invention has been described
5 in language more or less specific as to structural and methodical
6 features. It is to be understood, however, that the invention is not
7 limited to the specific features shown and described, since the means
8 herein disclosed comprise preferred forms of putting the invention into
9 effect. The invention is, therefore, claimed in any of its forms or
10 modifications within the proper scope of the appended claims
11 appropriately interpreted in accordance with the doctrine of equivalents.
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